

FORM PTO-892 (REV. 2-92)		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		SERIAL NO.	GROUP/ART UNIT 2505	ATTACHMENT TO PAGE NUMBER			
NOTICE OF REFERENCES CITED				APPLICANT(S) Tsang et al.					
				<div style="text-align: right;"> 3511 U.S. PATENT 09/14/99 08/31/98 </div>					
U.S. PATENT DOCUMENTS									
•		DOCUMENT NO.	DATE	NAME	CLASS	SUB-CLASS	FILING DATE IF APPROPRIATE		
	A	5,215,442	5/21/94	Belacqua et al.	257	350			
	B	4,917,028	4/5/90	Blanchard	257	353			
	C								
	D								
	E								
	F								
	G								
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	I								
	J								
	K								
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•		DOCUMENT NO.	DATE	COUNTRY	NAME	CLASS	SUB-CLASS	PERTINENT SHTS. DWG.	PP. SPEC.
	L	3,109,775	5/91	Japan	Sakamoto	257	302		
	M								
	N								
	O								
	P								
	Q								
OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)									
	R								
	S								
	T								
	U								
EXAMINER				DATE					
• A copy of this reference is not being furnished with this office action. (See Manual of Patent Examining Procedure, section 707.05 (a).)									

FORM PTO-892 (REV. 3-78)		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		SERIAL NO.	GROUP ART UNIT	ATTACHMENT TO PAPER NUMBER	
NOTICE OF REFERENCES CITED				APPLICANT(S) <i>D. Tsang et al</i>			

U.S. PAT. 14579
 10/28/98
 11/11/98

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•	A	B	C	D	E	F	G	H	I	J	K	DOCUMENT NO.	DATE	NAME	CLASS	SUI- CLASS	FILED DATE
*	A											5108427	8/92	<i>Tsai et al</i>	437	40	
*	B											4587712	5/86	<i>Salga</i>	437	6	
*	C											5089434	2/92	<i>Hollinger</i>	437	41	
*	D											5019522	5/91	<i>Meyer et al</i>	437	40	
*	E											4325073	4/82	<i>Hughes et al</i>	"	"	
*	F											5108937	4/92	<i>Tsai et al</i>	"	"	
*	G											4713358	12/87	<i>Bulat et al</i>	437	6	
*	H											4656076	4/87	<i>Vetanen et al</i>	437	41	
	I																
	J																
	K																

FOREIGN PATENT DOCUMENTS														
•	L	M	N	O	P	Q	DOCUMENT NO.	DATE	COUNTRY	NAME	CLASS	SUI- CLASS	PERTINENT SHEETS DWG.	PP. SPEC.
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•	<i>R Chang, Insulated Gate Bipolar Transistor (IGBT) with a Trench Gate Structure, IEDM Tech Digest, 1987, pp 674-677.</i>
•	<i>S Shenai, Optimum Low-Voltage Silicon Power Switches Fabricated Using Scaled Trench MOS Technologies, IEDM Tech Digest, 1991, pp 893-897.</i>
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•	<i>U Shenai, A 55-V, 0.2-m²-cm² Vertical Trench Power MOSFET, Electron Dev Lett, EDL-12, No 3, Mar 1991, pp 108-110.</i>

EXAMINER	DATE

* A copy of this reference is not being furnished with this office action.
 (See Manual of Patent Examination Procedure, Section 207.05 (a).)